BUDDHA INSTITUTE OF MANAGEMENT

DEPARTMENT OF COMPUTER APPLICATION

ACADEMIC YEAR 2025-26 (EVEN Semester)

LESSON PLAN

Semester: II	Section: A	Course Code: BBC-201	Contact Hours /week**: 5**
Course name: DIGITAL ELECTRONICS			# of credits: 4
Teacher's name: **Mr. Sudhir Shukla**			Designation: AP
Sessional Marks: 30		End Semester Examination Marks: 70	University Exam Hours: 3

Prerequisites if any:
NA

Content delivery methods:	By Face-to-Face delivery, Presentation, Tutorial etc.

COURSE SYLLABUS (as prescribed by University / Board)

Module No	UNIT Contents	Hours	COs
1	Binary Systems: Digital computers and Digital systems, Binary Numbers, Number Base conversion, Octal & Hexa-decimal numbers, Complements, Binary codes.	16	CO1
2	Boolean Algebra and Logic Gates: Basic definitions, Axiomatic definition, Basic theorems and Properties, Boolean Functions, Canonical and Standard Forms, Other Logic Operations, Digital Logic Gates.	16	CO2

3	Simplification of Boolean Functions: The Map method, two, three, four, five and six variable maps, Product of Sums and Sum of Products simplification, NAND and NOR implementation, Other two-level implementations, Don't-Care conditions, The Tabulation method, Determination and selection of Prime-Implicants.	14	CO3
4	Combinational Logic: Design procedure, Adders, Subtractors, Code conversion, Analysis procedure, Multilevel NAND and NOR circuits, Exclusive-OR and Equivalence Functions, Binary Parallel Adder, Decimal Adder, Magnitude comparator, Decoders, Multiplexers.	13	CO4
5	Sequential Logic, Registers and Counters: Flip-Flops, Triggering of Flip-Flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Flip-Flop Excitation Tables, Design procedure, Design of Counters, Design with State Equations, Registers, Shift Registers, Ripple Counters, Synchronous Counters, Timing Sequences.	15	CO5

COURSE OUTCOMES: At the end of the Course, the Student will be able to:

CO1	Apply concepts of Digital Binary System, complements and Binary codes.
CO2	Apply the concepts of Boolean Algebra and logic gates.
CO3	Understand and implementation of gates.
CO4	Analyze and Design of Combinational logic circuits.
CO5	Analysis and design sequential logic circuits with their applications. Implement the design procedure of synchronous and asynchronous sequential circuits.

Mapping of CO v/s PO:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	1	1	1	1	-	1	1	1	1
CO2	1	1	1	2	1	-	-	-	1	1	1	1
CO3	2	2	1	2	1	-	-	-	-	-	1	1
CO4	2	1	1	1	1	1	-	-	-	-	1	1
CO5	1	1	1	2	1	-	-	-	1	1	1	1
Average	1.4	1.2	1.0	1.6	1.0	0.4	0.2	-	0.6	0.6	1.2	1.4

	PSO1	PSO2	PSO3
CO1	2	1	1
CO2	2	1	1
CO3	2	1	1
CO4	2	1	1
CO5	2	1	1
Average	2	1	1

Correlation levels: 1-Slight (Low) 2-Moderate (Medium) 3-Substantial (High)

Gap in the syllabus	Topics related to array with function.

Topics to be covered beyond syllabus	Bridge topics which are helpful to explain concept of array passing to function.

LESSON PLAN-A

Lecture	Module	Scheduled				Conducted			
		Topic	*RBT Levels	C O Mapping	Date	Topic	Date	No. Of Students	Faculty Sign
1	I	**Binary Systems:** Introduction	K2	CO1					
2		**Binary Systems:** Introduction	K2						
3		Digital computers and Digital systems	K2						
4		Digital computers and Digital systems	K2						
5		Binary Numbers	K3						
6		Binary Numbers	K3						
7		Number Base conversion	K3						
8		Number Base conversion	K3						
9		**Tutorial-1**							
10		Number Base conversion	K3						
11		Octal & Hexa-decimal numbers	K3						
12		Octal & Hexa-decimal numbers	K3						

13		Complements	K3						
14		Complements	K3						
15		Binary codes	K3						
16		**Tutorial-2**							
17	II	**Boolean Algebra and Logic Gates:** Basic definitions	K3	CO2					
18		Boolean Algebra and Logic Gates: Axiomatic definition	K3						
19		Boolean Algebra and Logic Gates: Axiomatic definition	K3						
20		Basic theorems and Properties	K3						
21		Basic theorems and Properties	K3						
22		Basic theorems and Properties	K3						
23		Boolean Functions	K2						
24		Boolean Functions	K2						
25		**Tutorial-3**							
26		Canonical and Standard Forms	K2						
27		Canonical and Standard Forms	K2						

28		Canonical and Standard Forms	K2						
29		Other Logic Operations	K2						
30		Other Logic Operations	K2						
31		Digital Logic Gates	K2						
32		Digital Logic Gates	K2						
33		**Tutorial-4**							
34	III	**Simplification of Boolean Functions:**	K2						
35		Simplification of Boolean Functions:	K2						
36		The Map method							
37		**The Map method** two, three, four, five and six variable maps	K2						
38		The Map method two, three, four, five and six variable maps	K3						
39		Product of Sums and Sum of Products simplification	K3						
40		Product of Sums and Sum of Products simplification	K3						
41		**Tutorial-5**							
42		NAND and NOR implementation	K2						
43		Other two-level implementations	K2						

44		Other two-level implementations	K2						
45		Don’t-Care conditions	K2						
46		The Tabulation method	K2						
47		Determination and selection of Prime-Implicants.	K3						
48		**Tutorial-6**							
49	IV	**Combinational Logic: Design procedure**	K2	CO4					
50		Combinational Logic: Design procedure	K2						
51		Combinational Logic: Design procedure	K2						
52		Adders	K2						
53		Subtractors	K2						
54		Code conversion	K2						
55		Analysis procedure	K2						
56		**Tutorial-7**	K2						
57		Multilevel NAND and NOR circuits	K2						
58		Exclusive-OR and Equivalence Functions	K2						

59		Decimal Adder	K2						
60		Magnitude comparator	K2						
61		Decoders, Multiplexers	K2						
62		**Tutorial-8**							
63	V	**Sequential Logic, Registers and Counters: Flip-Flops**	K2	CO5					
64		Triggering of Flip-Flops, Analysis of Clocked Sequential Circuits							
65		State Reduction and Assignment	K2						
66		Flip-Flop Excitation Tables	K2						
67		**Tutorial-9**							
68		**Design of Counters**	K2						
69		Design with State Equations	K2						
70		Registers, Shift Registers	K2						
71		Ripple Counters	K2						
72		Synchronous Counters, Timing Sequences	K2						
73		**Tutorial-10**							

74		Revision							
75		Revision							

Class Test	Syllabus
CT-01	1-24 class
CT-02	24-50
PRE-AKTU	Full Syllabus

***Revised Bloom's Taxonomy (RBT) Levels:**
L1 – Remembering; L2 – Understanding; L3 – Applying; L4 – Analysing; L5 – Evaluating; L6 - Creating

References:
Text books :(As per University / Board syllabus)

T1. Mano M., "Digital Design", Prentice-Hall of India.

T2. Gaur R.K., "Digital Electronics and Micro-computers", Dhanpat Rai Publications.

Reference Books:(As per University / Board syllabus)

R1. Rajaraman V. and Radhakrishanan T., "An Introduction to Digital Computer Design", Prentice-Hall India Pvt. Ltd

R2. Gill N.S. and Dixit J.B, "Digital Design & Computer Organization", University Science Press.

Faculty Sign **HOD's sign**